PARALLEL FRACTIONAL INTERPOLATOR WITH DATA-RATE CLOCK SYNCHRONIZATION

ABSTRACT OF THE DISCLOSURE

A circuit for single or parallel digital fractional interpolation of data samples has a fractional interpolator filter, an oscillator for outputting timing signals to the fractional interpolator filter, and a detector loop with a strobe feedback from the oscillator for outputting a frequency adjustment to the oscillator. Three different approaches are shown to determine the frequency adjustment. One approach is to generate a pulse based on the symbol clock, and measure the differences between the pulse and the strobe and between the strobe and the pulse. The smaller is the frequency adjustment. Another approach is to adjust the strobe period to match the symbol clock period. A third approach is to add an oscillator-driven clock to the symbol clock and integrate the sum over a symbol clock period to generate the frequency adjustment. Preferably, the interpolator filter takes N parallel inputs and samples each in parallel based on a plurality of oscillator timing signals, each corrected with reference to the frequency adjustment.